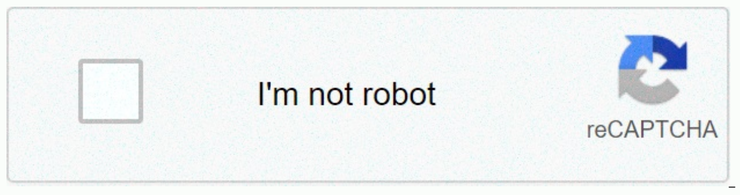

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According to The Yanalog to Digital Converters (ADC), the signal translates real world signals like temperature, pressure, quality, current, distance, or light intensity into a digital representation. This digital can be represented then executed, distorted, counted, transferred or stored. Figure 20.1 According to digital conversions in many cases, the digital conversion process is just one step within a large measurement and control-up of the control-up where digitalized data is implemented and then rechanged on the Yanalog signal to run external transformers. These transformers include things like motors, heters and voice like loudspeakers. The performance of the ADC requirement will reflect the performance objectives of measurement and control of the lupe. ADC performance requirements will also reflect the capabilities and needs of other signal processing elements in the loup. The Chitra 20.2 measurement and control-the-lobe uniform an ADC sample slot assign a single-time interval to waveform and a digital price on each sample. The digital value appears on the production of converter in a winery coded form. The sample by price reference value is achieved by the distribution of the Yanalog input-input-value and multiplied by the number of digital codes they have. The converter solution is set by the number of binary bits in the output code. Chatra 20.3 Digital Output Code is an ADC two process, sample dispersal and wanton. ADC represents a yanalog signal, which has unlimited resolution that contains a digital code that has limited resolution. ADC produces 2N digital values where N represents the number of binary production bits. The Input Signal will fall between the level of the contasion because the converter has made a limited resolution as a result of a inherited uncertainty or contasion error. This error determines the maximum dynamic range of converter. The Chatra 20.4 contasion process represents a continuous time domain signal to the sample process in which the passive and uniform with the scale values at the interval of time. The sample in this process determines the maximum bandwidth of the signal in which The Nycist theory is consistent. This rule states that signal frequency must be less than or equal to a half sample to prevent ilaisang. Ilyasang is a condition in which the frequency signal outside the required signal band appears inside it through the sample process. Of interest. However, this Ilyasang process can be exploited in changing a high frequency signal at low frequency in the design of the communication system. It is known as the model under technology. Below is a quality for sample that aDC has enough input bandwidth and dynamic range to get the most frequency signal of interest. Data 20.5 sample stake process sample suo-tonnization and countasation are important concepts because they set an ideal ADC performance range. In an ideal ADC, code transaction is exactly 1 less important butt (lsb) plus. Therefore, for a n-bit ADC, there are 2N codes and 1 LSB = FS/2N, where FS is full-scale Input-Input-Value. However, real-world ADC operation is also affected by unprecedented effects, which create mistakes beyond those imposed by converter solutions and sample rates. These errors are revealed in a large number of AC and DC performance specifications associated with ADCs. Shape 20.6 Transition Function provides an ideal ADC-same digital output code in any of the input in this range. Details and conditions, Myasuremenangsaganafakanka DC's explanations represent a yanalog signal of solutions or bit units, usually 6 to 24. Determines how small input can be resolved. The conversion speed or rate, ksamples/s or Msamples/number of changes per second time for a full-scale change explains the specific resolution and ability of The Leech Itya to take the fastest sample stake adc's least important bit (LSB) right most bits in an ADC output code. LSB size is a function of the converter solution. Not a specific, but a general term. The most important bit (MSB) is the left most bit in an ADC output code. Not a specific, but a general term. The difference appears in the non-fit (DGL), the terms of deviation from the lsbithi (LSB 1) code width between any two close codes. In an ideal converter, each code is exactly the same size and the DML is zero. Get dgl,, offset error, and error that represents signals across the internal and external ranges of data. Integrated Non-Related (Inal), described in the LSB terms (also known as the relative accuracy error) is dispersion of an original code transfer point from its ideal position on a straight line prepared between the end points of the transfer function. Due to the extent of width of the code can lead to low or wide missing codes and include noise and frequency spurs out of the effects of the quantasation. Offset, when the converter input is zero, the difference between ideal and original production is stated in terms of the difference. explains the absolute accuracy of the converter. After the offset and the errors are removed. Get error/full scale error, in a terms of expression the difference between the LSB ideal and the actual output when the converter input is full scale. The inal frequency creates additional harmonacs and spurs in the domain. Chitra 20.7 DGL with ADC transfer event Chatra 20.8 ADC transfer works with the details and conditions of error, Myasuremenangsaganafakanka AC Specification Fake Free Dynamic Range (Sfdor), dBThe ratio of the largest fake signal in The Bandwidth to its fundamental frequency length. Important in communication applications where one can interfere with a fork channel. Total regular average deformity (tad), dBThe ratio of the rms amount of the first six hermonax to the length of frequency. The noise related to haramonax are ingredients, or by creation, from a-d conversion. The Haramonacs can limit the dynamic performance of the converter. Signal to Noise to Desid Ratio (INAD), dBThe signal ratio except for the basic amount of all other workman components including Haramonax- at the cost of the meaning of RSO. Their ad indicates that this 2nd and 3rd Hramonax effective number is included in the effects of butts (ENOB) ... ENOB 1.76 dB 6.02 explains the dynamic performance of a The ADC compared to an ideal converter. Signal to noise ratio (SNR) or signal to noise ratio without haramonax. Like AnAD, rms signal ratio is first the five except The Ramonax and DC, like the dimensions of all other workman components at the cost of the basic amount-squares of the meaning. SNER indicates the noise performance of a converter compared to an ideal converter. The Yanalog bandwidth (full strength, small signal), kilogram or input frequency where the OUTPUT of FFT is basically 3 dB. Usually set by converter samples and hold-up softener. Important applications under sample stake. This report cannot be compatible with the ADC's maximum sample stake rate. Consumption of electricity, mw or use of converted power. Important power sensitive applications in which battery life, temperature, or space ranges can affect the needs of power consumption. The Chatra 20.9 Frequency Domain Specification speed and accuracy are two important steps of ADC performance. Thus, they provide a means for wide ranking for today's adCs. ADC chips can be in groups with these lines as common objectives, fast or health related. Converters with 8-to-14-bit resolution and conversion rates are generally considered common purpose ADCs. With conversion rates above 10 Msamples/S, these people usually get the fast nickname, while with them fall from 16 bits or more resolution to the health-related ADC category. However, these definitions reflect somewhat autonomous and mostly the art of the present state. Within these wide ranges, ADCs can also be grouped according to converter architecture. The most popular types are Flash, Papayaanad, Continuous Callia Register, and L'Kdelta. Each architecture provides some benefits in terms of speed, accuracy, and other parameters of conversion. Features attached to each architecture Determine its relevance to a given application. ADCs have both never been built with hybrid packaging and have been applicable as integrated circuits (ICs) as applicable akhand designs. Most of the adc performance discussion within these pages is specifically related to Adc in the DCC form. The development process of adCs has been heavily influenced by innovation, both end processes such as the biopooler, bakamos, and SiGe, as well as the cmos process centrally. Over time, the transition of ADC design to cmos process with

small jams has increased the chances of increased performance, while the high level of integration also allows. This integration can increase the number of conversion channels achieved on the same death, or allow conversion-related functions to keep quiet. As a result, the size of the die and consequently, the size of the package depends on the process of semi-mucosal. This process also determines the supply-quality, which, along with the speed of conversion, influences the consumption of electricity. In flash or parallel ADC architecture, a row of 2N-1 comparisons replaces a yanalog signal for digital with a resolution of N bits. Compare one input and get the yanalog signal on a unique part of the reference-vultage on the other. For each comparison, the reference vultage is often a tap from a humorous vultage-pall, with comparisons as neutral in increasing the 1 stls of the same quality. Compare saini together is the clockad. Compared with the lower reference than the Input, The Yanalog will be a digital one product. The Yanalog input will output a digital zero with more than t-age reference comparison. After reading with each other, the results offer a thermometer code in which the output logic changes to standard winery code. Chitra 20.10 Flash-R:+ converts very quickly into an ADC clock cycle. Con:- Many comparisons are required. The physical limitations of the akhand integration usually only allow 8 bits of an ADC chip resolution. -High input input This architecture divides conversions into two or more stages. Each stage consists of sample and hold (S/H) circuit, an m-bit flash ADC, and a D. Yanalog signal is fed in the first phase, where it is sampled by S/H and the flash is converted into a digital code by ADC. The flash code generated by The ADC in this phase represents the most important bits of the final production of ADC. The same code is then fed to d, which converts the code back to a yanalog signal that is the original, sample dismounted from the Yanalog input signal. As a result the difference signal or the sesame, is amplified next and sent to the pipeline at the following stage, where the entire process is repeated. The number of steps needed depends on the required resolution and the flash ADCs resolution used in each stage. In theory, the total ADC resolution resolutions will amount to ADCs but in practice, some extra overlap bits are needed to correct the error. Pros: + Pure flash architecture not as fast as fast, but get higher resolutions and dynamic range. + Handle the widebond pit. + Dither enhances the effective solution of noise use and convertconverted converter. + Signal under permits if taking widebrand samples. Kans:- Pipeline delay. The total rate may be equal to a flash converter (one change per cycle), but with equal to a number of dimensions or pipeline delays. - The accuracy of conversion depends on labour. -Fit for sick-applications where conversion results must be available immediately after the sample clock. The Chitra 20.11 Single Papayaanad Converter Phase Head Converter works like a balance scale that compares an unknown weight against the series of known weights. In return for weight, sir converter compares the Input Wallet selves against a series of continuously small-mahi NT representing each of the bits in the digital output code. These fishing fractions are full-scale input-wallets (1/2, 1/4, 1/8, 1/16... 1/2N, where N = number of bits). The first comparison is created between the Input Wallet and a Wallet representing the most important bit (MSB). If this is higher than the Input-Input-Value MSB-Value, the PRICE OF MSB is set to 1, otherwise it is set to 0. The second comparison is created between The Yanalog Input Wallet and a Vultage REPRESENTING MSB and the next most important bit amount. The second most important bit value is set accordingly. The third comparison is made up of the input-input-walletage and the total amount of three most important bits. At this time, the third most important bit value is set. Re-presents the process as long as the lsb price is set up. Pros: + Akhand uses a comparison to get higher resolution as a result of small die size for ADCs. + No pipeline delays. + Well suited for non-meadadi put. + Dither enhances the effective solution of noise use and convertconverted converter. + Under Permission. The N-comparison is required to get the con-n-bit resolution, which is higher than both Flash and Papalad. - Depending on the accuracy of the conversion and the comparison noise. Chitra 20.12 Continuous Lyon-Register (Head) ADC The basic elements of this architecture are an interterter, a comparison, and a one-bit, one-to-one form as one with each other-delta dispersal. The appendenditis to the subretitus input signal and then the signal feed to the intitor. The output of the interter is a comparison, which converts the signal into a one-bit digital product. The result is a little d fed, which produces a yanalog signal to be dismounted from the input signal. This process reintroduces at the rate of over-suppallad very fast. The supplement produces a river of winery with a function of the ratio of the xerus The length and breadth of the signal. By digital filtering and another zero of this river Dekamattang, the value of the Yanalog input is represented by a winery yield. Pros: + The most health-related production for low-input-bandwidth applications. + Allows in which low frequency is transferred to higher frequency in the form of noise, outside of the band of interest. + Oversampalling reduces the requirements for anti-ilyasang filtering. Con:-Print is much higher than other archetextures. -Oversampalling and printing after the disputing molatoplugin input signals-discourage the use of Delta ADCs. Go to the previous chapter on Delta Architecture by Chitra 20.13 See list for going to the next chapter: University/Courses/Electronics/Text/chapter-20 .txt · Last Modified: 05 Sep 2013 19:55 By Damrkar Damrkar